National Semiconductor

August 1, 2008

ADC102S101
2 Channel, 500 ksps to 1 Msps, 10-Bit A/D Converter

General Description

The ADC102S101 is a low-power, two-channel CMOS 10-bit analog-to-digital converter with a high-speed serial interface. Unlike the conventional practice of specifying performance at a single sample rate only, the ADC102S101 is fully specified over a sample rate range of 500 ksps to 1 Msps. The converter is based on a successive-approximation register architecture with an internal track-and-hold circuit. It can be configured to accept one or two input signals at inputs IN1 and IN2.

The output serial data is straight binary, and is compatible with several standards, such as SPI™, QSPI™, MICROWIRE, and many common DSP serial interfaces.

The ADC102S101 operates with a single supply that can range from +2.7V to +5.25V. Normal power consumption using a +3V or +5V supply is 3.9 mW and 11.4 mW, respectively. The power-down feature reduces the power consumption to just 0.12 µW using a +3.6V supply, or 0.47 µW using a +5.5V supply.

The ADC102S101 is packaged in an 8-lead MSOP package. Operation over the industrial temperature range of −40°C to +85°C is guaranteed.

Features

- Specified over a range of sample rates.
- Two input channels
- Variable power management
- Single power supply with 2.7V - 5.25V range

Key Specifications

- DNL + 0.26/−0.16 LSB (typ)
- INL + 0.4/−0.1 LSB (typ)
- SNR 61.7 dB (typ)
- Power Consumption
- — 3V Supply 3.9 mW (typ)
  — 5V Supply 11.4 mW (typ)

Applications

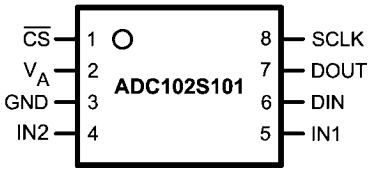
- Portable Systems
- Remote Data Acquisition
- Instrumentation and Control Systems

Pin-Compatible Alternatives by Resolution and Speed

All devices are fully pin and function compatible.

Resolution	Specified for Sample Rates of:		
	50 to 200 ksps	**200 to 500 ksps**	**500 ksps to 1 Msps**
12-bit	ADC122S021	ADC122S051	ADC122S101
10-bit	ADC102S021	ADC102S051	**ADC102S101**
8-bit	ADC082S021	ADC082S051	ADC082S101

Connection Diagram



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Ordering Information

Order Code	Temperature Range	Description	Top Mark
ADC102S101CIMM	−40°C to +85°C	8-Lead MSOP Package	X23C
ADC102S101CIMMX	−40°C to +85°C	8-Lead MSOP Package, Tape & Reel	X23C
ADC102S101EVAL		Evaluation Board	

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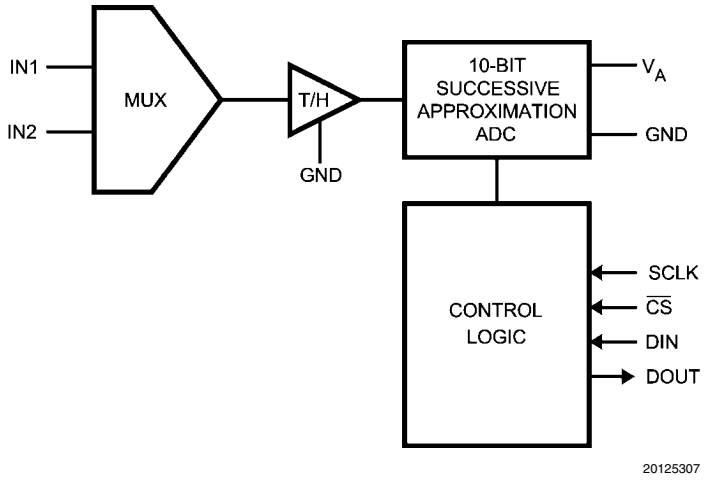
Block Diagram



Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Description
ANALOG I/O		
5,4	IN1 and IN2	Analog inputs. These signals can range from 0V to V_A.
DIGITAL I/O		
8	SCLK	Digital clock input. This clock directly controls the conversion and readout processes.
7	DOUT	Digital data output. The output samples are clocked out of this pin on falling edges of the SCLK pin.
6	DIN	Digital data input. The ADC102S101's Control Register is loaded through this pin on rising edges of the SCLK pin.
1	$\overline{CS}$	Chip select. On the falling edge of $\overline{CS}$, a conversion process begins. Conversions continue as long as $\overline{CS}$ is held low.
POWER SUPPLY		
2	V_A	Positive supply pin. This pin should be connected to a quiet +2.7V to +5.25V source and bypassed to GND with a 1 µF capacitor and a 0.1 µF monolithic capacitor located within 1 cm of the power pin.
3	GND	The ground return for the die.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Analog Supply Voltage V_A	−0.3V to 6.5V
Voltage on Any Pin to GND	−0.3V to V_A +0.3V
Input Current at Any Pin (Note 3)	±10 mA
Package Input Current (Note 3)	±20 mA
Power Consumption at T_A = 25°C	See (Note 4)
ESD Susceptibility (Note 5)	
Human Body Model	2500V
Machine Model	250V
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C

Operating Ratings (Notes 1, 2)

Operating Temperature Range	−40°C ≤ T_A ≤ +85°C
V_A Supply Voltage	+2.7V to +5.25V
Digital Input Pins Voltage Range	−0.3V to V_A
Clock Frequency	0.8 to 16 MHz
Analog Input Voltage	0V to V_A

Package Thermal Resistance

Package	θ_{JA}
8-lead MSOP	250°C / W

Soldering process must comply with National Semiconductor's Reflow Temperature Profile specifications. Refer to www.national.com/packaging. (Note 6)

ADC102S101 Converter Electrical Characteristics (Note 9)

The following specifications apply for V_A = +2.7V to 5.25V, GND = 0V, C_L = 50 pF, f_{SCLK} = 8 MHz to 16 MHz, f_{SAMPLE} = 500 ksps to 1 Msps, unless otherwise noted. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**: all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Typical	Limits (Note 7)	Units
STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes			**10**	Bits
INL	Integral Non-Linearity		+0.4	**+0.7**	LSB (max)
			−0.1	**−0.5**	LSB (min)
DNL	Differential Non-Linearity		+0.26	**+0.6**	LSB (max)
			−0.16	**−0.6**	LSB (min)
V_{OFF}	Offset Error		+0.19	**±0.6**	LSB (max)
OEM	Channel to Channel Offset Error Match		0.02	**±0.6**	LSB (max)
FSE	Full-Scale Error		−0.15	**±0.7**	LSB (max)
FSEM	Channel to Channel Full-Scale Error Match		0.02	**±0.5**	LSB (max)
DYNAMIC CONVERTER CHARACTERISTICS					
SINAD	Signal-to-Noise Plus Distortion Ratio	V_A = +2.7V to 5.25V f_{IN} = 40.3 kHz, −0.02 dBFS	61.6	**61**	dB (min)
SNR	Signal-to-Noise Ratio	V_A = +2.7V to 5.25V f_{IN} = 40.3 kHz, −0.02 dBFS	61.7	**61.3**	dB (min)
THD	Total Harmonic Distortion	V_A = +2.7V to 5.25V f_{IN} = 40.3 kHz, −0.02 dBFS	−82	**−72**	dB (max)
SFDR	Spurious-Free Dynamic Range	V_A = +2.7V to 5.25V f_{IN} = 40.3 kHz, −0.02 dBFS	83	**75**	dB (min)
ENOB	Effective Number of Bits	V_A = +2.7V to 5.25V f_{IN} = 40.3 kHz, −0.02 dBFS	9.9	**9.8**	Bits (min)
	Channel-to-Channel Crosstalk	V_A = +5.25V f_{IN} = 40.3 kHz	−78		dB
IMD	Intermodulation Distortion, Second Order Terms	V_A = +5.25V f_a = 40.161 kHz, f_b = 41.015 kHz	−82		dB
	Intermodulation Distortion, Third Order Terms	V_A = +5.25V f_a = 40.161 kHz, f_b = 41.015 kHz	−81		dB
FPBW	-3 dB Full Power Bandwidth	V_A = +5V	11		MHz
		V_A = +3V	8		MHz

Symbol	Parameter	Conditions	Typical	Limits (Note 7)	Units
ANALOG INPUT CHARACTERISTICS					
V_{IN}	Input Range		0 to V_A		V
I_{DCL}	DC Leakage Current			**±1**	µA (max)
C_{INA}	Input Capacitance	Track Mode	33		pF
		Hold Mode	3		pF
DIGITAL INPUT CHARACTERISTICS					
V_{IH}	Input High Voltage	V_A = +5.25V		**2.4**	V (min)
		V_A = +3.6V		**2.1**	V (min)
V_{IL}	Input Low Voltage			**0.8**	V (max)
I_{IN}	Input Current	V_{IN} = 0V or V_A	±0.2	**±10**	µA (max)
C_{IND}	Digital Input Capacitance		2	**4**	pF (max)
DIGITAL OUTPUT CHARACTERISTICS					
V_{OH}	Output High Voltage	I_{SOURCE} = 200 µA	V_A – 0.03	**V_A – 0.5**	V (min)
		I_{SOURCE} = 1mA	V_A – 0.1		V
V_{OL}	Output Low Voltage	I_{SINK} = 200 µA	0.03	**0.4**	V (max)
		I_{SINK} = 1 mA	0.1		V
I_{OZH}, I_{OZL}	TRI-STATE® Leakage Current		±0.01	**±1**	µA (max)
C_{OUT}	TRI-STATE® Output Capacitance		2	**4**	pF (max)
	Output Coding		Straight (Natural) Binary		
POWER SUPPLY CHARACTERISTICS (C_L = 10 pF)					
V_A	Supply Voltage			**2.7**	V (min)
				5.25	V (max)
I_A	Supply Current, Normal Mode (Operational, $\overline{CS}$ low)	V_A = +5.25V, f_{SAMPLE} = 1 Msps, f_{IN} = 40 kHz	2.18	**2.7**	mA (max)
		V_A = +3.6V, f_{SAMPLE} = 1 Msps, f_{IN} = 40 kHz	1.08	**1.3**	mA (max)
	Supply Current, Shutdown ($\overline{CS}$ high)	V_A = +5.25V, f_{SAMPLE} = 0 ksps	90		nA
		V_A = +3.6V, f_{SAMPLE} = 0 ksps	33		nA
P_D	Power Consumption, Normal Mode (Operational, $\overline{CS}$ low)	V_A = +5.25V	11.4	**14.2**	mW (max)
		V_A = +3.6V	3.9	**4.7**	mW (max)
	Power Consumption, Shutdown ($\overline{CS}$ high)	V_A = +5.25V	0.47		µW
		V_A = +3.6V	0.12		µW
AC ELECTRICAL CHARACTERISTICS					
f_{SCLK}	Clock Frequency	(Note 8)		**8**	MHz (min)
				16	MHz (max)
f_S	Sample Rate	(Note 8)		**500**	ksps (min)
				1	Msps (max)
t_{CONV}	Conversion Time			**13**	SCLK cycles
DC	SCLK Duty Cycle	f_{CLK} = 16 MHz	50	**30**	% (min)
				70	% (max)
t_{ACQ}	Track/Hold Acquisition Time	Full-Scale Step Input		**3**	SCLK cycles
	Throughput Time	Acquisition Time + Conversion Time		**16**	SCLK cycles

ADC102S101 Timing Specifications

The following specifications apply for V_A = +2.7V to 5.25V, GND = 0V, C_L = 50 pF, f_{SCLK} = 8 MHz to 16 MHz, f_{SAMPLE} = 500 ksps to 1 Msps, **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**: all other limits T_A = 25°C.

Symbol	Parameter	Conditions		Typical	Limits (Note 7)	Units
t_{CSU}	Setup Time SCLK High to $\overline{CS}$ Falling Edge	(Note 10)	V_A = +3.0V	–3.5	**10**	ns (min)
			V_A = +5.0V	–0.5		
t_{CLH}	Hold time SCLK Low to $\overline{CS}$ Falling Edge	(Note 10)	V_A = +3.0V	+4.5	**10**	ns (min)
			V_A = +5.0V	+1.5		
t_{EN}	Delay from $\overline{CS}$ Until DOUT active		V_A = +3.0V	+4	**30**	ns (max)
			V_A = +5.0V	+2		
t_{ACC}	Data Access Time after SCLK Falling Edge		V_A = +3.0V	+16.5	**30**	ns (max)
			V_A = +5.0V	+15		
t_{SU}	Data Setup Time Prior to SCLK Rising Edge			+3	**10**	ns (min)
t_H	Data Valid SCLK Hold Time			+3	**10**	ns (min)
t_{CH}	SCLK High Pulse Width			0.5 x t_{SCLK}	**0.3 x t_{SCLK}**	ns (min)
t_{CL}	SCLK Low Pulse Width			0.5 x t_{SCLK}	**0.3 x t_{SCLK}**	ns (min)
t_{DIS}	$\overline{CS}$ Rising Edge to DOUT High-Impedance	Output Falling	V_A = +3.0V	1.7	**20**	ns (max)
			V_A = +5.0V	1.2		
		Output Rising	V_A = +3.0V	1		
			V_A = +5.0V	1		

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND = 0V, unless otherwise specified.

Note 3: When the input voltage at any pin exceeds the power supply (that is, V_{IN} < GND or V_{IN} > V_A), the current at that pin should be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two. The Absolute Maximum Rating specification does not apply to the V_A pin. The current into the V_A pin is limited by the Analog Supply Voltage specification.

Note 4: The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A)/\theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

Note 5: Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through zero ohms

Note 6: Reflow temperature profiles are different for lead-free and non-lead-free packages.

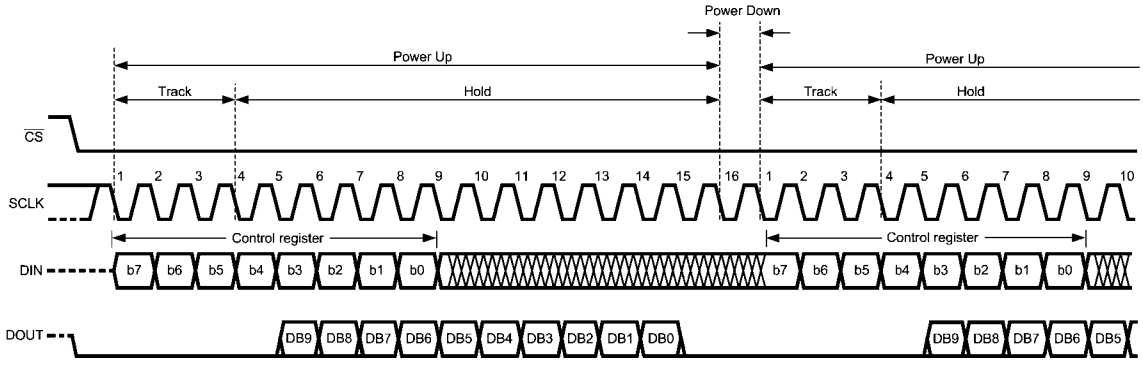
Note 7: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: This is the frequency range over which the electrical performance is guaranteed. The device is functional over a wider range which is specified under Operating Ratings.

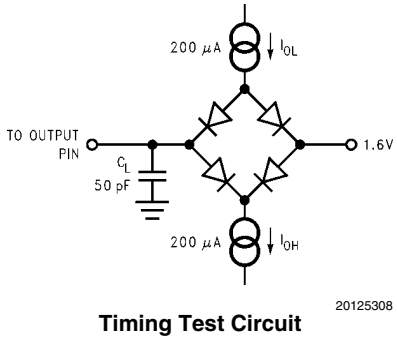
Note 9: Min/max specification limits are guaranteed by design, test, or statistical analysis.

Note 10: Clock may be either high or low when $\overline{CS}$ is asserted as long as setup and hold times t_{CSU} and t_{CLH} are strictly observed.

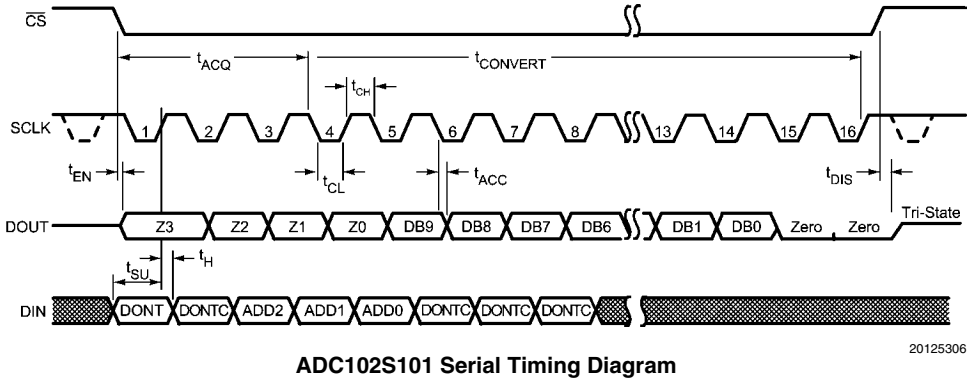
Timing Diagrams



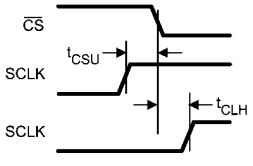
ADC102S101 Operational Timing Diagram



Timing Test Circuit



ADC102S101 Serial Timing Diagram



SCLK and $\overline{CS}$ Timing Parameters

Specification Definitions

ACQUISITION TIME is the time required to acquire the input voltage. That is, it is time required for the hold capacitor to charge up to the input voltage.

APERTURE DELAY is the time between the fourth falling SCLK edge of a conversion and the time when the input signal is acquired or held for conversion.

CONVERSION TIME is the time required, after the input voltage is acquired, for the ADC to convert the input voltage to a digital word.

CROSSTALK is the coupling of energy from one channel into the other channel, or the amount of signal energy from one analog input that appears at the measured analog input.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD – 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

FULL SCALE ERROR (FSE) is a measure of how far the last code transition is from the ideal 1½ LSB below V_{REF+} and is defined as:

$$V_{FSE} = V_{max} + 1.5\ LSB - V_{REF+}$$

where V_{max} is the voltage at which the transition to the maximum code occurs. FSE can be expressed in Volts, LSB or percent of full scale range.

GAIN ERROR is the deviation of the last code transition (111...110) to (111...111) from the ideal (V_{REF} – 1.5 LSB), after adjusting for offset error.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the second and third order intermodulation products to the sum of the power in both of the original frequencies. IMD is usually expressed in dB.

MISSING CODES are those output codes that will never appear at the ADC outputs. These codes cannot be reached with any input value. The ADC102S101 is guaranteed not to have any missing codes.

OFFSET ERROR is the deviation of the first code transition (000...000) to (000...001) from the ideal (i.e. GND + 0.5 LSB).

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal at the converter output to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including d.c. or harmonics included in the THD specification..

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal where a spurious signal is any signal present in the output spectrum that is not present at the input, excluding d.c.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB or dBc, of the rms total of the first five harmonic components at the output to the rms level of the input signal frequency as seen at the output. THD is calculated as

$$THD = 20 \cdot \log_{10} \sqrt{\frac{A_{f2}^2 + \cdots + A_{f6}^2}{A_{f1}^2}}$$

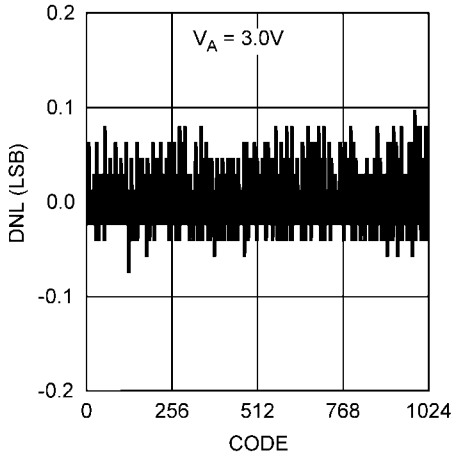
where Af_1 is the RMS power of the input frequency at the output and Af_2 through Af_6 are the RMS power in the first 5 harmonic frequencies. Accurate THD measurement requires a spectrally pure sine wave (monotone) at the ADC input.

THROUGHPUT TIME is the minimum time required between the start of two successive conversion. It is the acquisition time plus the conversion time. In the case of the ADC102S101, this is 16 SCLK periods.

Typical Performance Characteristics

T_A = +25°C, f_{SAMPLE} = 500 ksps to 1 Msps, f_{SCLK} = 8 MHz to 16 MHz, f_{IN} = 40.3 kHz unless otherwise stated.

DNL - V_A = 3.0V



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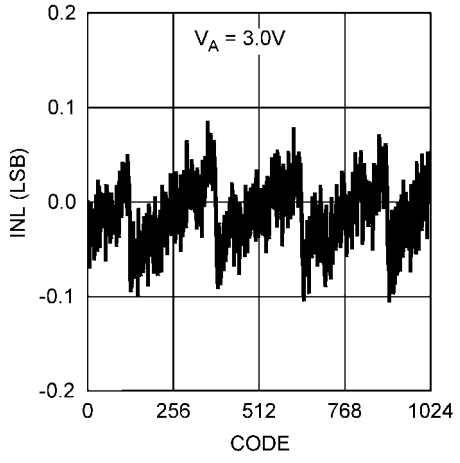
INL - V_A = 3.0V



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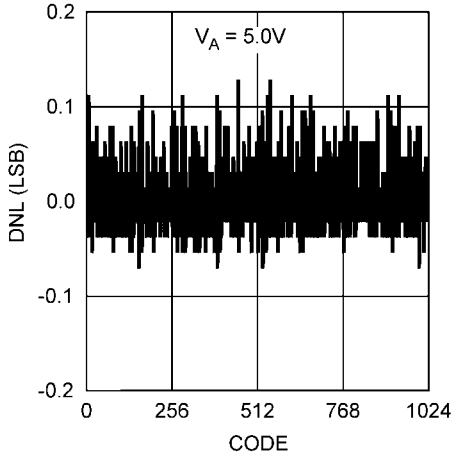
DNL - V_A = 5.0V



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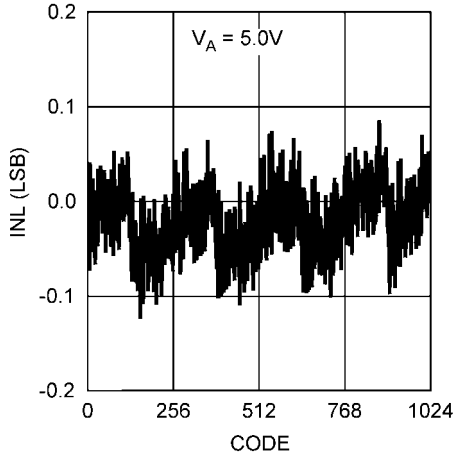
INL - V_A = 5.0V



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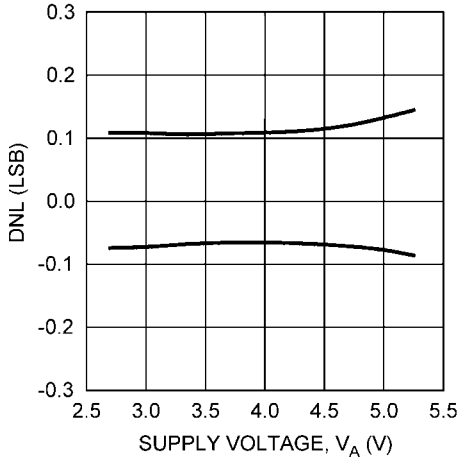
DNL vs. Supply



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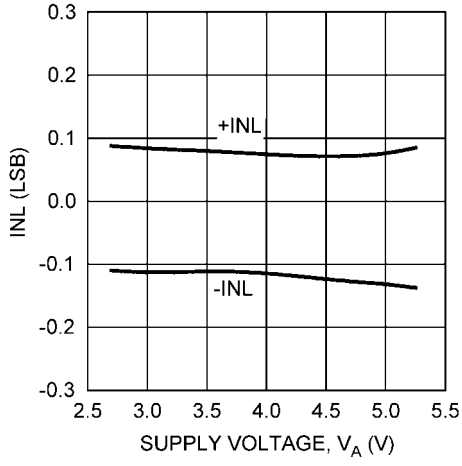
INL vs. Supply



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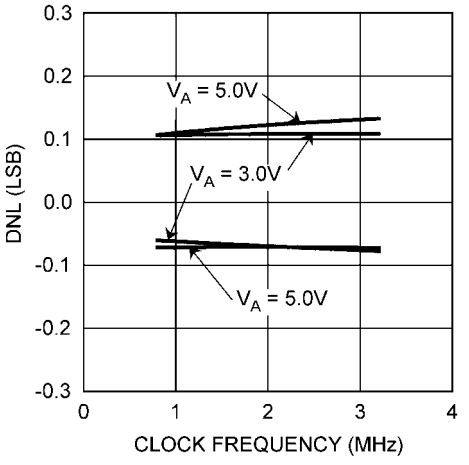
DNL vs. Clock Frequency



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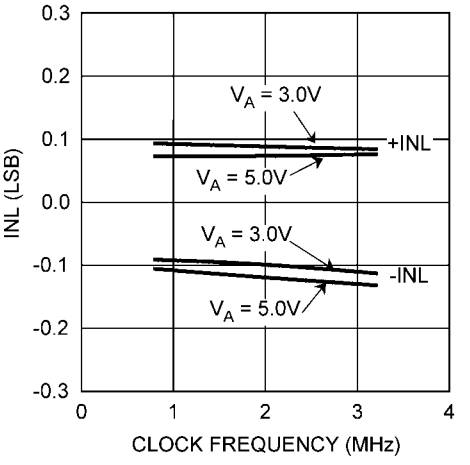
INL vs. Clock Frequency



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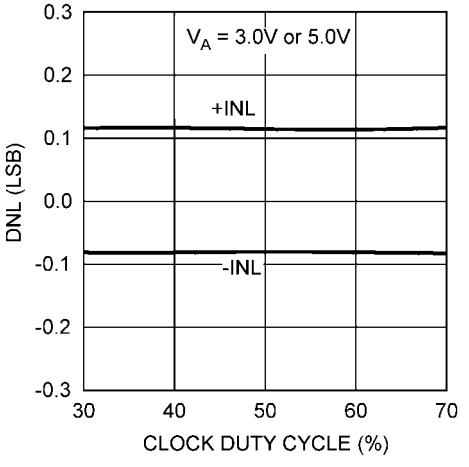
DNL vs. Clock Duty Cycle



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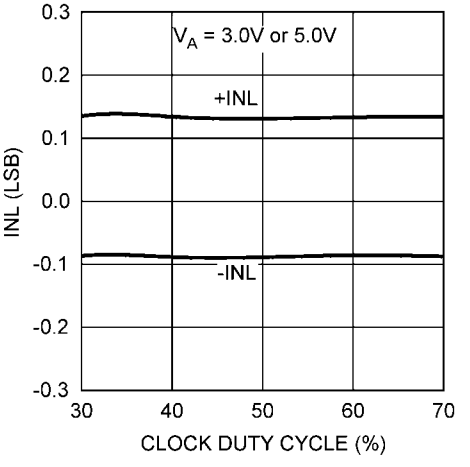
INL vs. Clock Duty Cycle



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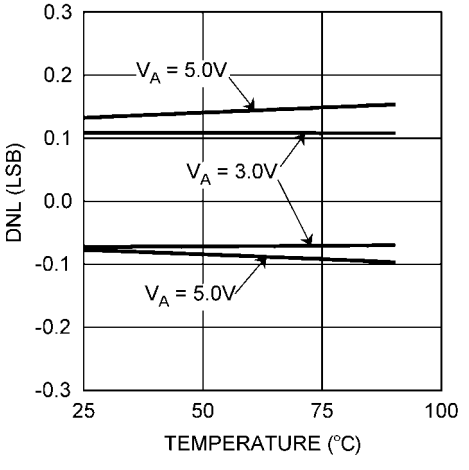
DNL vs. Temperature



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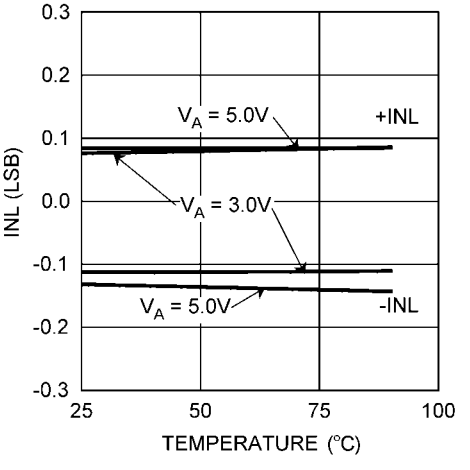
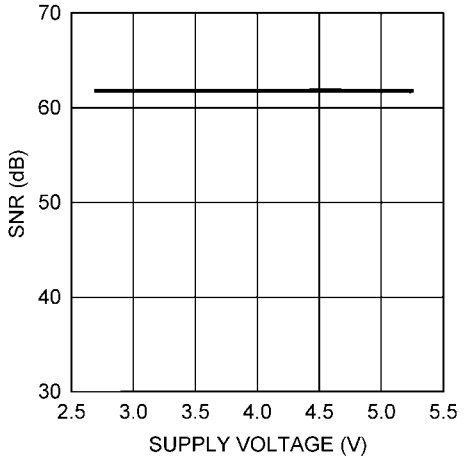
INL vs. Temperature



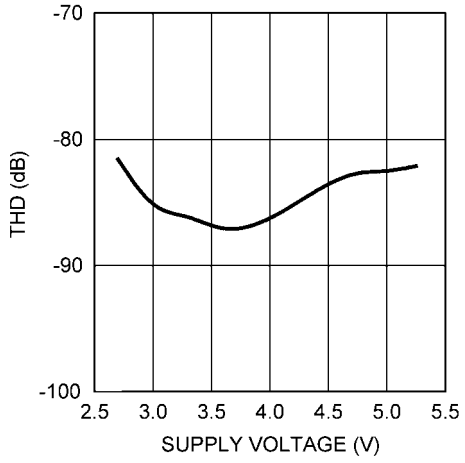
20125329

SNR vs. Supply



20125330

THD vs. Supply



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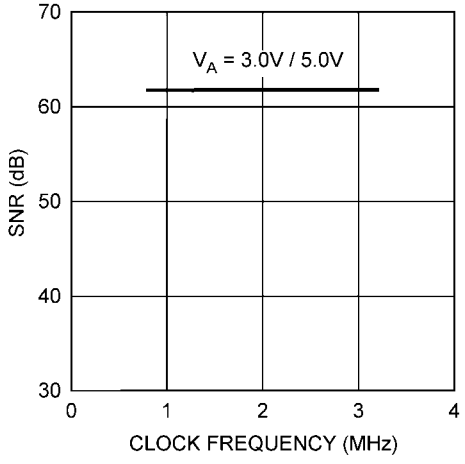
SNR vs. Clock Frequency



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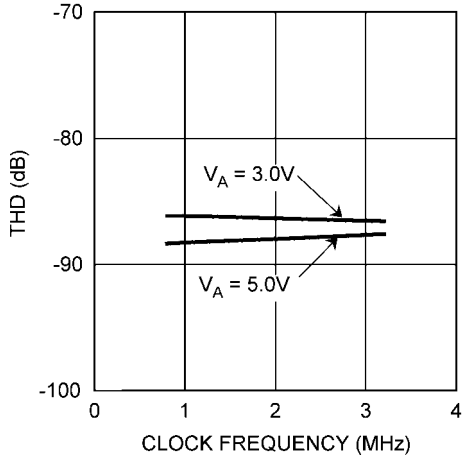
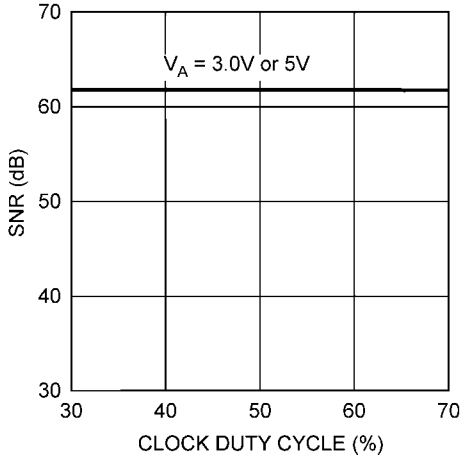
THD vs. Clock Frequency



20125336

SNR vs. Clock Duty Cycle



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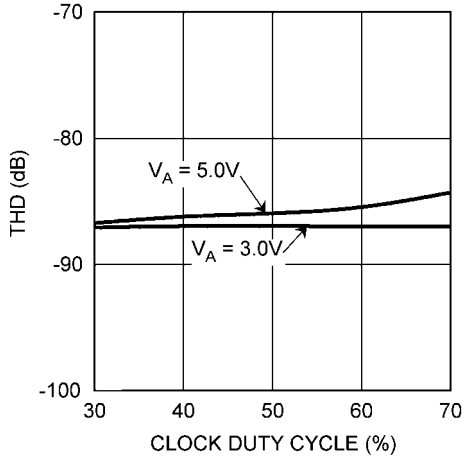
THD vs. Clock Duty Cycle



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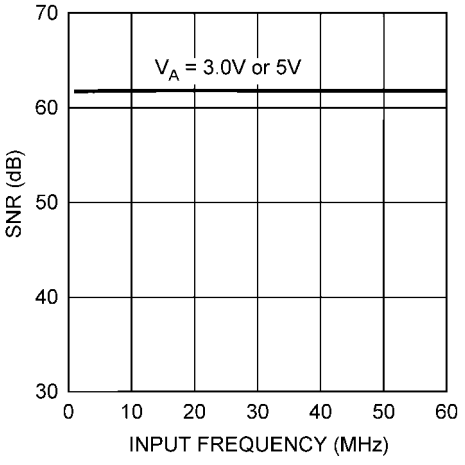
SNR vs. Input Frequency



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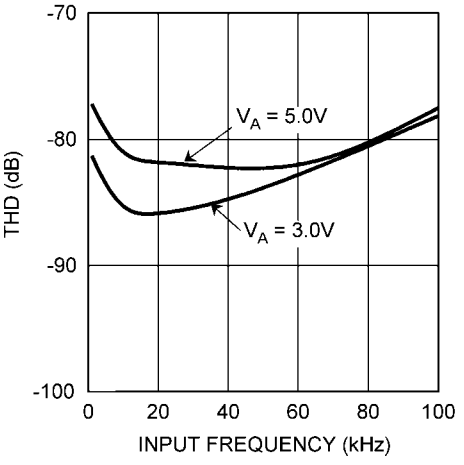
THD vs. Input Frequency



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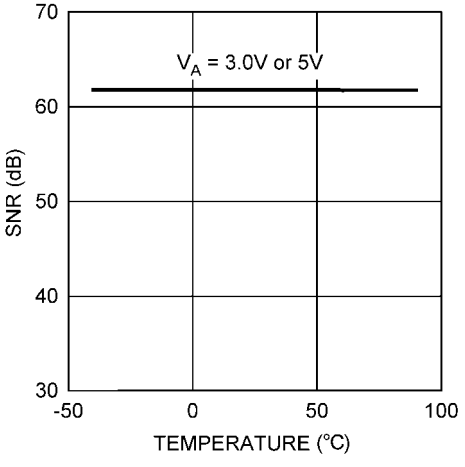
SNR vs. Temperature



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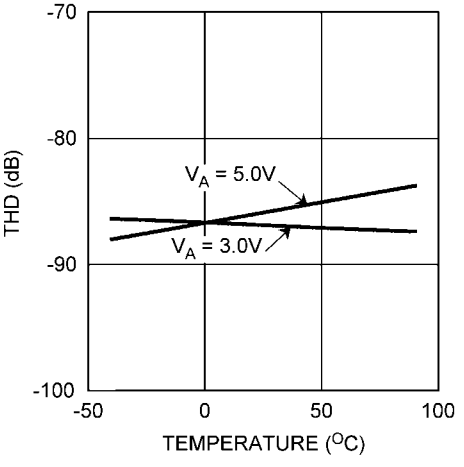
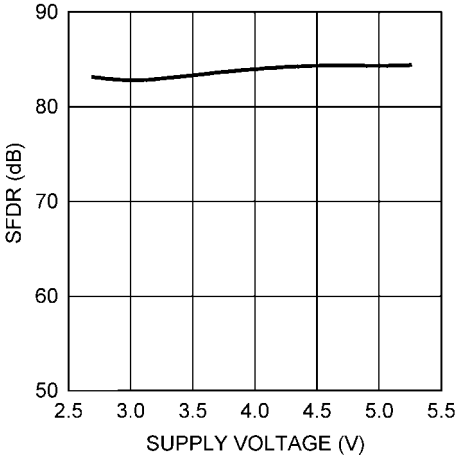
THD vs. Temperature



20125339

SFDR vs. Supply



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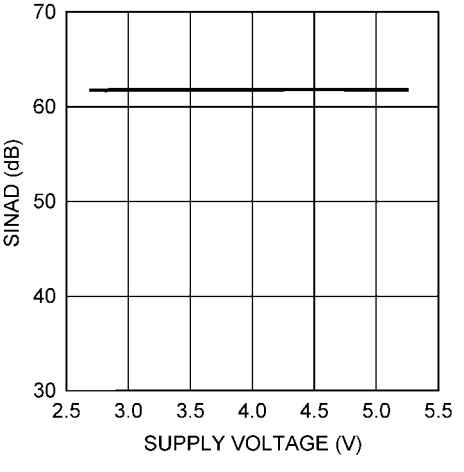
SINAD vs. Supply



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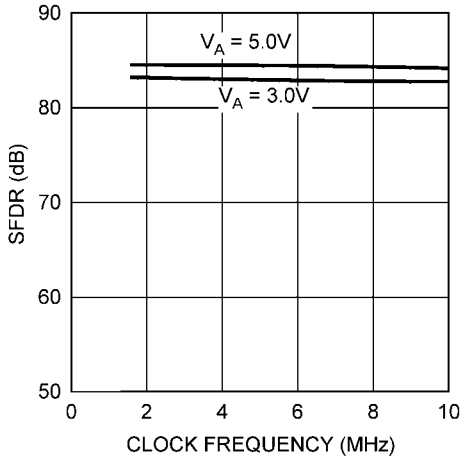
SFDR vs. Clock Frequency



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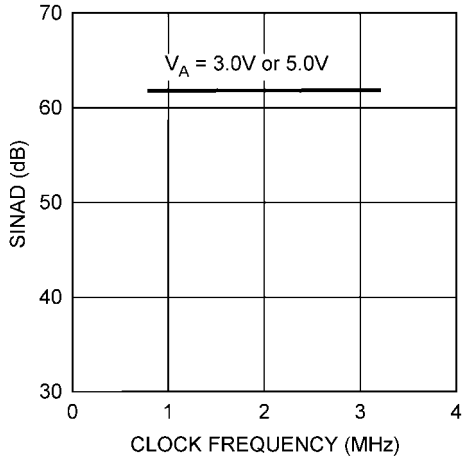
SINAD vs. Clock Frequency



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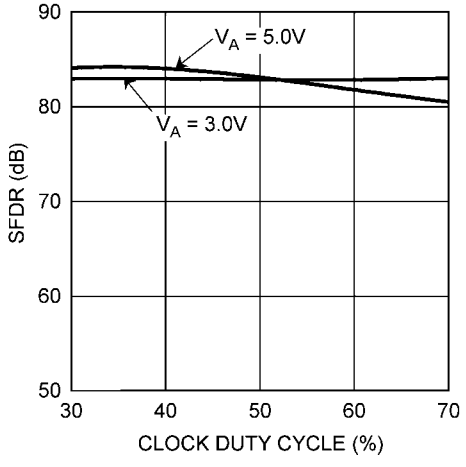
SFDR vs. Clock Duty Cycle



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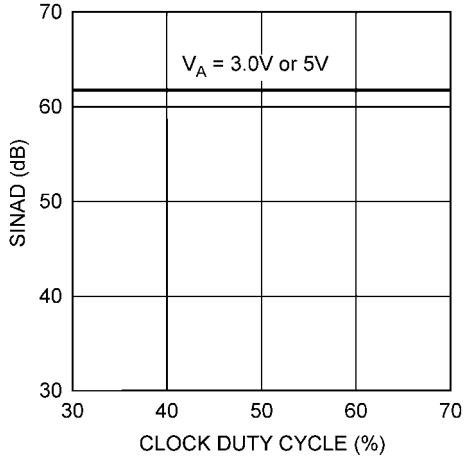
SINAD vs. Clock Duty Cycle



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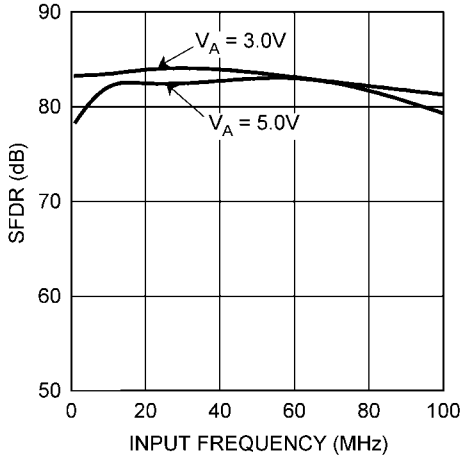
SFDR vs. Input Frequency



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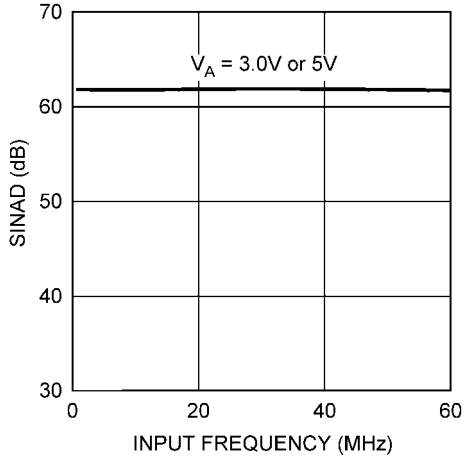
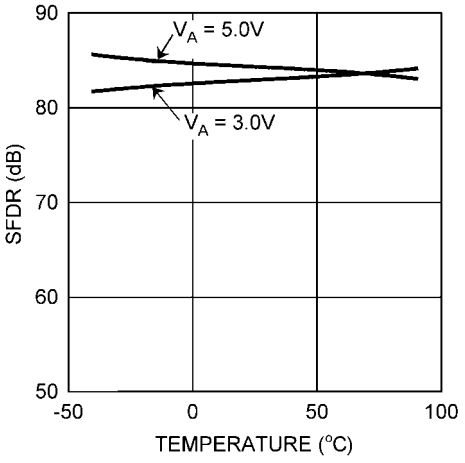
SINAD vs. Input Frequency



20125348

SFDR vs. Temperature



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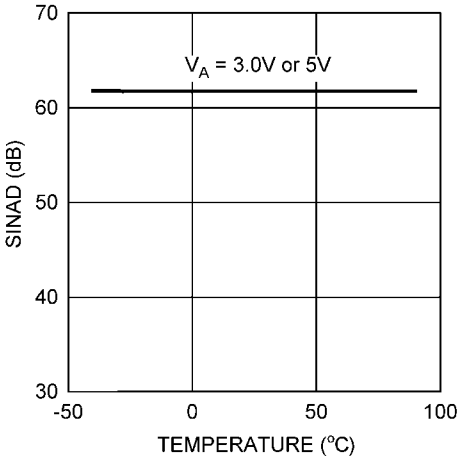
SINAD vs. Temperature



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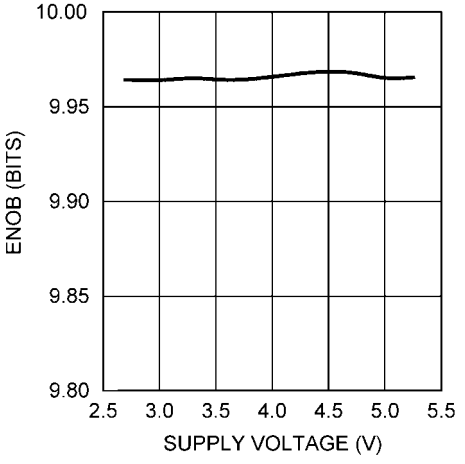
ENOB vs. Supply



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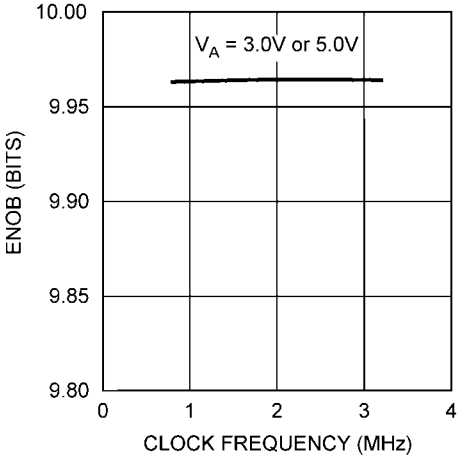
ENOB vs. Clock Frequency



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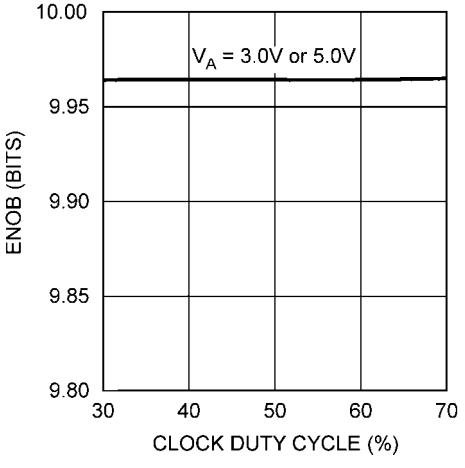
ENOB vs. Clock Duty Cycle



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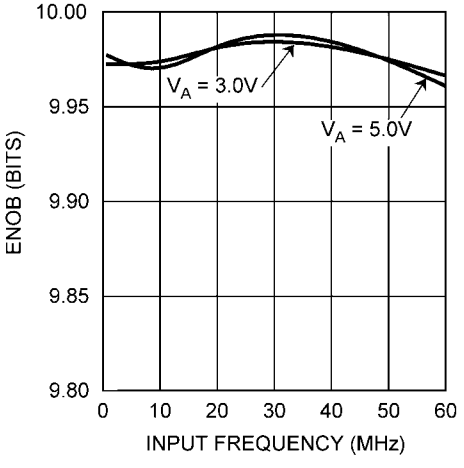
ENOB vs. Input Frequency



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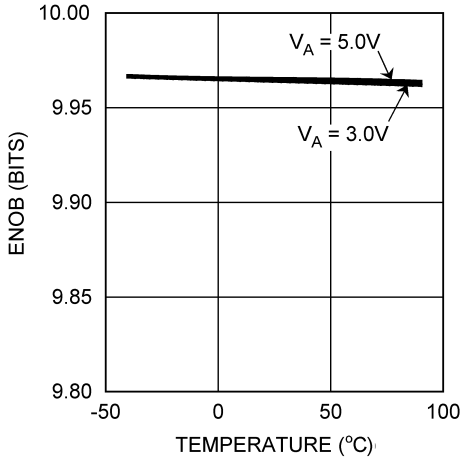
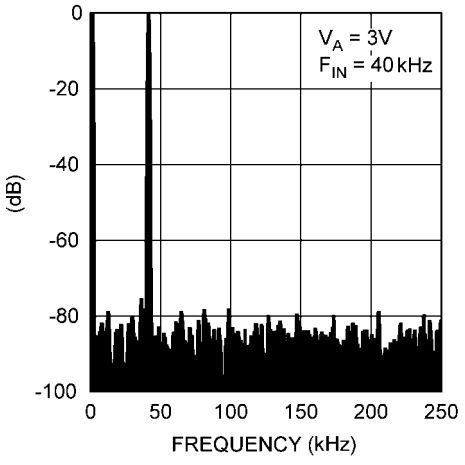


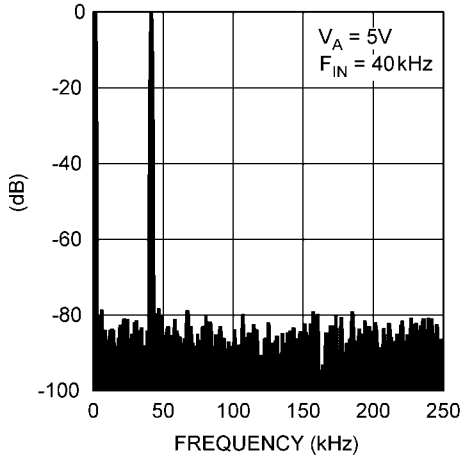
20125356

Spectral Response - 3V, 500 ksps



20125364

Spectral Response - 5V, 500 ksps



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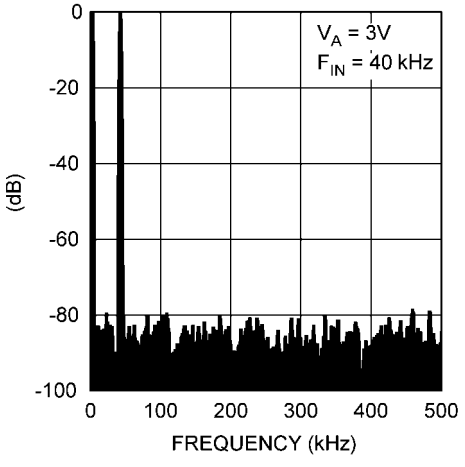
Spectral Response - 3V, 1.0 Msps



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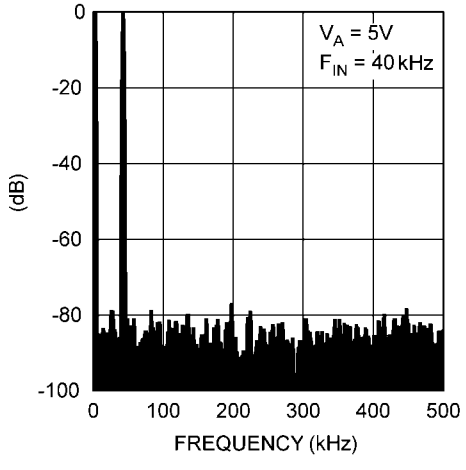
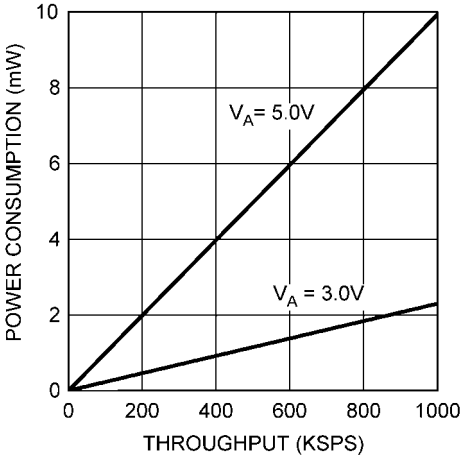
Spectral Response - 5V, 1.0 Msps



20125360

Power Consumption vs. Throughput



20125361

Applications Information

1.0 ADC102S101 OPERATION

The ADC102S101 is a successive-approximation analog-to-digital converter designed around a charge-redistribution digital-to-analog converter. Simplified schematics of the ADC102S101 in both track and hold modes are shown in *Figures 1*, *2*, respectively. In *Figure 1*, the ADC102S101 is in track mode: switch SW1 connects the sampling capacitor to one of two analog input channels through the multiplexer, and SW2 balances the comparator inputs. The ADC102S101 is in this state for the first three SCLK cycles after $\overline{CS}$ is brought low.

Figure 2 shows the ADC102S101 in hold mode: switch SW1 connects the sampling capacitor to ground, maintaining the sampled voltage, and switch SW2 unbalances the comparator. The control logic then instructs the charge-redistribution DAC to add fixed amounts of charge to the sampling capacitor until the comparator is balanced. When the comparator is balanced, the digital word supplied to the DAC is the digital representation of the analog input voltage. The ADC102S101 is in this state for the fourth through sixteenth SCLK cycles after $\overline{CS}$ is brought low.

The time when $\overline{CS}$ is low is considered a serial frame. Each of these frames should contain an integer multiple of 16 SCLK cycles, during which time a conversion is performed and clocked out at the DOUT pin and data is clocked into the DIN pin to indicate the multiplexer address for the next conversion.

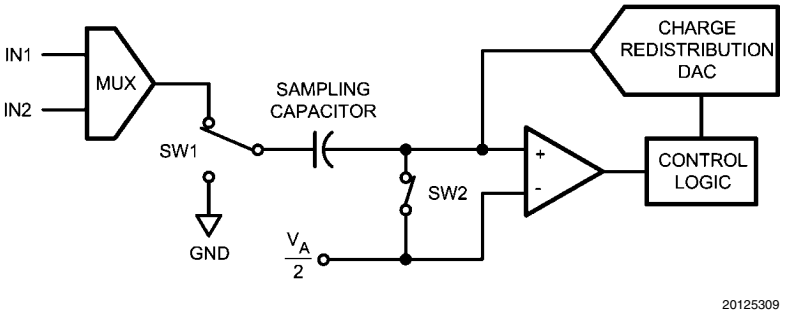


FIGURE 1. ADC102S101 in Track Mode

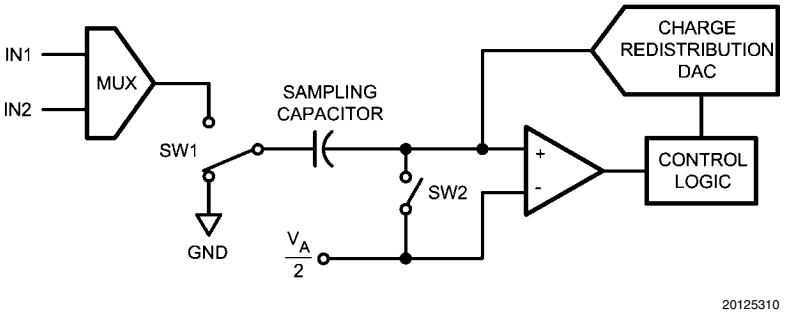


FIGURE 2. ADC102S101 in Hold Mode

2.0 USING THE ADC102S101

An ADC102S101 timing diagram and a serial interface timing diagram for the ADC102S101 are shown in the Timing Diagrams section. $\overline{CS}$ is chip select, which initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. DOUT is the serial data output pin, where a conversion result is sent as a serial data stream, MSB first. Data to be written to the ADC102S101's Control Register is placed at DIN, the serial data input pin. New data is written to DIN with each conversion.

A serial frame is initiated on the falling edge of $\overline{CS}$ and ends on the rising edge of $\overline{CS}$. Each frame must contain an integer multiple of 16 rising SCLK edges. The ADC output data (DOUT) is in a high impedance state when $\overline{CS}$ is high and is active when $\overline{CS}$ is low. Thus, $\overline{CS}$ acts as an output enable. Additionally, the device goes into a power down state when $\overline{CS}$ is high and also between continuous conversion cycles.

During the first 3 cycles of SCLK, the ADC is in the track mode, acquiring the input voltage. For the next 13 SCLK cycles the conversion is accomplished and the data is clocked out, MSB first, starting at the 5th clock. If there is more than one conversion in a frame, the ADC will re-enter the track mode on the falling edge of SCLK after the N*16th rising edge of SCLK, and re-enter the hold/convert mode on the N*16+4th falling edge of SCLK, where "N" is an integer.

When $\overline{CS}$ is brought high, SCLK is internally gated off. If SCLK is stopped in the low state while $\overline{CS}$ is high, the subsequent fall of $\overline{CS}$ will generate a falling edge of the internal version of SCLK, putting the ADC into the track mode. This is seen by the ADC as the first falling edge of SCLK. If SCLK is stopped with SCLK high, the ADC enters the track mode on the first falling edge of SCLK after the falling edge of $\overline{CS}$.

During each conversion, data is clocked into the ADC at DIN on the first 8 rising edges of SCLK after the fall of $\overline{CS}$. For each conversion, it is necessary to clock in the data indicating

the input that is selected for the conversion after the current one. See *Tables 1*, *2* and *Table 3*.

If $\overline{CS}$ and SCLK go low within the times defined by t_{CSU} and t_{CLH}, the rising edge of SCLK that begins clocking data in at DIN may be one clock cycle later than expected. It is, therefore, best to strictly observe the minimum t_{CSU} and t_{CLH} times given in the Timing Specifications.

There are no power-up delays or dummy conversions required with the ADC102S101. The ADC is able to sample and convert an input to full conversion immediately following power up. The first conversion result after power-up will be that of IN1.

TABLE 1. Control Register Bits

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DONTC	**DONTC**	**ADD2**	**ADD1**	**ADD0**	**DONTC**	**DONTC**	**DONTC**

TABLE 2. Control Register Bit Descriptions

Bit #:	**Symbol:**	**Description**
7 - 6, 2 - 0	DONTC	Don't care. The value of these bits do not affect the device.
3	ADD0	These bits determine which input channel will be sampled and converted in the next track/hold cycle. The mapping between codes and channels is shown in *Table 3*.
4	ADD1	
5	ADD2	

TABLE 3. Input Channel Selection

ADD2	**ADD1**	**ADD0**	**Input Channel**
x	0	0	IN1 (Default)
x	0	1	IN2
x	1	x	Not allowed. The output signal at the D_{OUT} pin is indeterminate if ADD1 is high.

3.0 ADC102S101 TRANSFER FUNCTION

The output format of the ADC102S101 is straight binary. Code transitions occur midway between successive integer LSB values. The LSB width for the ADC102S101 is V_A/1024. The ideal transfer characteristic is shown in *Figure 3*. The transition from an output code of 00 0000 0000 to a code of 00 0000 0001 is at 1/2 LSB, or a voltage of V_A/2048. Other code transitions occur at steps of one LSB.

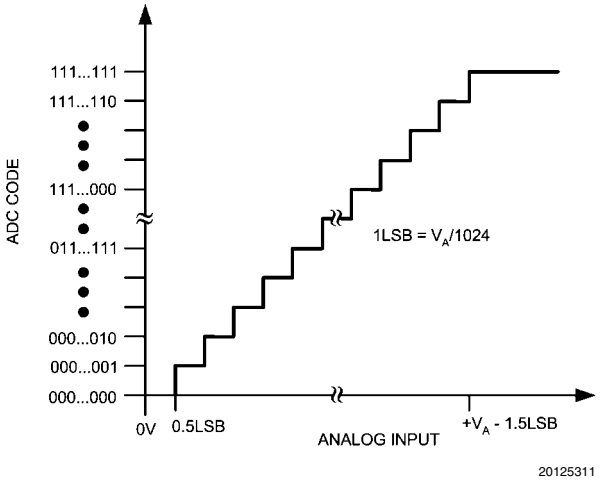


FIGURE 3. Ideal Transfer Characteristic

4.0 TYPICAL APPLICATION CIRCUIT

A typical application of the ADC102S101 is shown in *Figure 4*. Power is provided, in this example, by the National Semiconductor LP2950 low-dropout voltage regulator, available in a variety of fixed and adjustable output voltages. The power supply pin is bypassed with a capacitor network located close to the ADC102S101. Because the reference for the ADC102S101 is the supply voltage, any noise on the supply will degrade device noise performance. To keep noise off the supply, use a dedicated linear regulator for this device, or provide sufficient decoupling from other circuitry to keep noise off the ADC102S101 supply pin. Because of the ADC102S101's low power requirements, it is also possible to use a precision reference as a power supply to maximize performance. The four-wire interface is shown connected to a microprocessor or DSP.

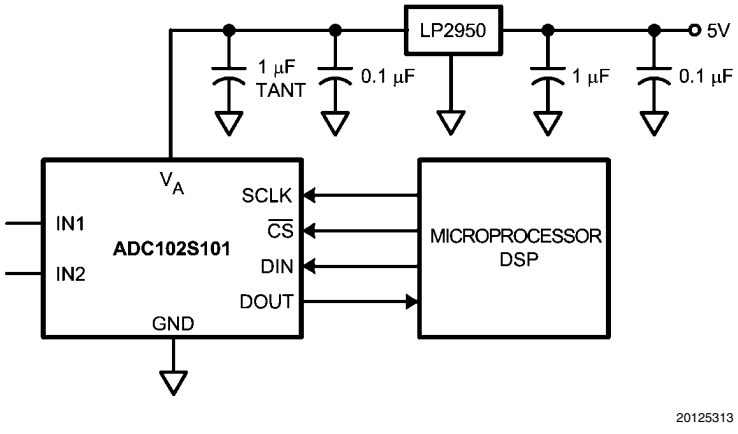


FIGURE 4. Typical Application Circuit

5.0 ANALOG INPUTS

An equivalent circuit for one of the ADC102S101's input channels is shown in *Figure 5*. Diodes D1 and D2 provide ESD protection for the analog inputs. At no time should any input go beyond (V_A + 300 mV) or (GND – 300 mV), as these ESD diodes will begin conducting, which could result in erratic operation. For this reason, these ESD diodes should NOT be used to clamp the input signal.

The capacitor C1 in *Figure 5* has a typical value of 3 pF, and is mainly the package pin capacitance. Resistor R1 is the on resistance of the multiplexer and track / hold switch, and is typically 500 ohms. Capacitor C2 is the ADC102S101 sampling capacitor and is typically 30 pF. The ADC102S101 will deliver best performance when driven by a low-impedance source to eliminate distortion caused by the charging of the sampling capacitance. This is especially important when using the ADC102S101 to sample AC signals. Also important when sampling dynamic signals is a band-pass or low-pass filter to reduce harmonics and noise, improving dynamic performance.

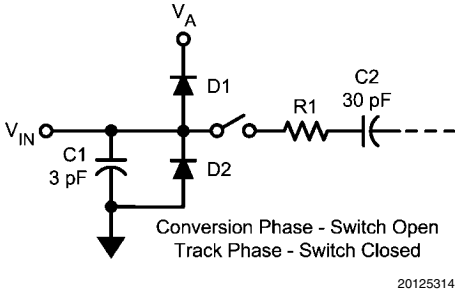


FIGURE 5. Equivalent Input Circuit

6.0 DIGITAL INPUTS AND OUTPUTS

The ADC102S101's digital output DOUT is limited by, and cannot exceed, the supply voltage, V_A. The digital input pins are not prone to latch-up and, and although not recommended, SCLK, $\overline{CS}$ and DIN may be asserted before V_A without any latchup risk.

7.0 POWER SUPPLY CONSIDERATIONS

The ADC102S101 is fully powered-up whenever $\overline{CS}$ is low, and fully powered-down whenever $\overline{CS}$ is high, with one exception: the ADC102S101 automatically enters power-down mode between the 16th falling edge of a conversion and the 1st falling edge of the subsequent conversion (see Timing Diagrams).

The ADC102S101 can perform multiple conversions back to back; each conversion requires 16 SCLK cycles. The ADC102S101 will perform conversions continuously as long as $\overline{CS}$ is held low.

The user may trade off throughput for power consumption by simply performing fewer conversions per unit time. The Power Consumption vs. Sample Rate curve in the Typical Performance Curves section shows the typical power consumption of the ADC102S101 versus throughput. To calculate the power consumption, simply multiply the fraction of time spent in the normal mode by the normal mode power consumption , and add the fraction of time spent in shutdown mode multiplied by the shutdown mode power dissipation.

7.1 Power Supply Noise Considerations

The charging of any output load capacitance requires current from the power supply, V_A. The current pulses required from the supply to charge the output capacitance will cause voltage variations on the supply. If these variations are large enough, they could degrade SNR and SINAD performance of the ADC. Furthermore, discharging the output capacitance when the digital output goes from a logic high to a logic low will dump current into the die substrate, which is resistive. Load discharge currents will cause "ground bounce" noise in the substrate that will degrade noise performance if that current is large enough. The larger is the output capacitance, the more current flows through the die substrate and the greater is the noise coupled into the analog channel, degrading noise performance.

To keep noise out of the power supply, keep the output load capacitance as small as practical. If the load capacitance is greater than 50 pF, use a 100 Ω series resistor at the ADC output, located as close to the ADC output pin as practical. This will limit the charge and discharge current of the output capacitance and improve noise performance.

7.2 Power Supply Noise Considerations

The charging of any output load capacitance requires current from the power supply, V_A. The current pulses required from the supply to charge the output capacitance will cause voltage variations on the supply. If these variations are large enough, they could degrade SNR and SINAD performance of the ADC. Furthermore, discharging the output capacitance when the digital output goes from a logic high to a logic low will dump current into the die substrate, which is resistive. Load discharge currents will cause "ground bounce" noise in the substrate that will degrade noise performance if that current is large enough. The larger is the output capacitance, the more current flows through the die substrate and the greater is the noise coupled into the analog channel, degrading noise performance.

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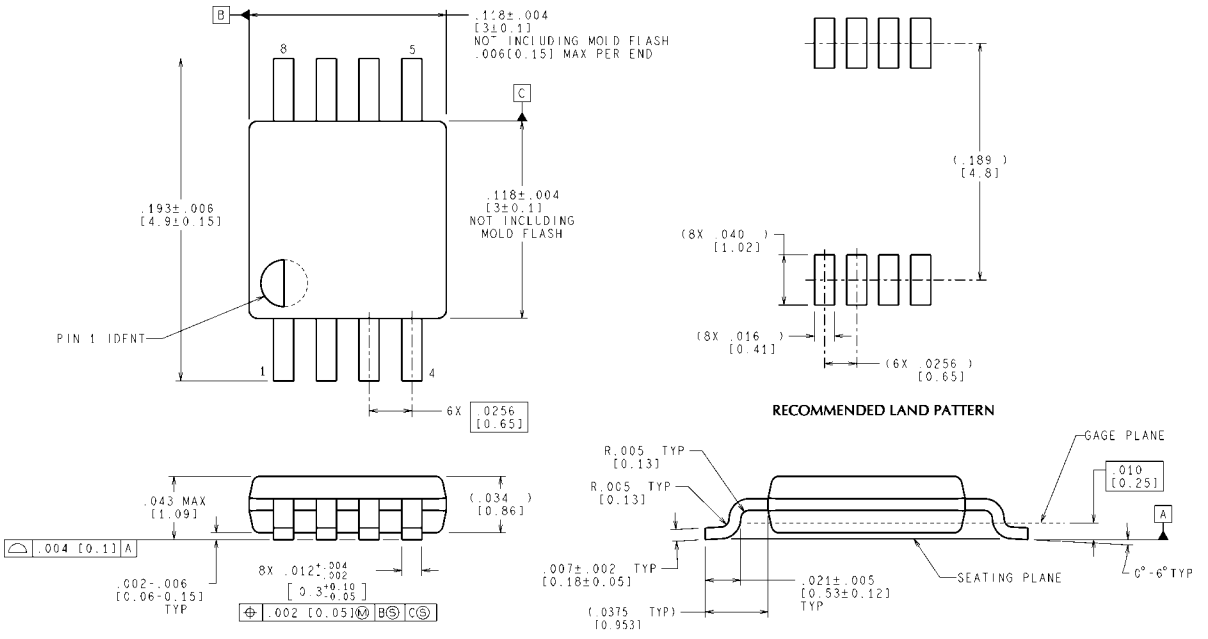
Physical Dimensions inches (millimeters) unless otherwise noted



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MUA08A (Rev F)

8-Lead MSOP
Order Number ADC102S101CIMM, ADC102S101CIMMX
NS Package Number P0MUA08A

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